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EXAMINER	
FLOURNOY, HORACE L	
ART UNIT	**PAPER NUMBER**
2189	

DATE MAILED: 03/27/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/787,444	BACCHUS, REZA MUSHTAG	
	Examiner	Art Unit	
	Horace L. Flournoy	2189	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *26 February 2004*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-28* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-28* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *26 February 2004* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date *2/26/2004*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

The instant application having Application No. **10/787,444** has a total of *28* claims pending in the application; there are *7* independent claims and *21* dependent claims, all of which are ready for examination by the examiner.

ACKNOWLEDGEMENT OF REFERENCES CITED BY APPLICANT

As required by **M.P.E.P.** 609(c), the applicant's submission of the Information Disclosure Statement dated **2/26/2004** is acknowledged by the examiner and the cited references have been considered in the examination of the claims now pending. As required by **M.P.E.P.** 609(c), a copy of the PTOL-1449 initialed and dated by the examiner is attached to the instant office action.

INFORMATION CONCERNING OATH/DECLARATION

Oath/Declaration

The applicant's oath/declaration has been reviewed by the examiner and is found to conform to the requirements prescribed in **37 C.F.R. 1.63**.

REJECTIONS BASED ON PRIOR ART

Claim Rejections - 35 USC § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless –

(b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

Claims 1-28 are rejected under 35 U.S.C. 102(b) as being anticipated by **Herring et al. (U.S Patent No. 5,860,081 hereafter referred to as Herring)**.

With respect to **independent claim 1,**

"A computer system, comprising: a central processing unit ("CPU"); **[FIG. 1, element 14: "CPU Core"]** *a bridge device coupled to a main memory;* **[FIG. 1, elements 26: as interpreted by the examiner, these devices are a bridge device which is coupled to main memory ("System Memory" 36)]** *a cache controller coupled between the bridge device and the CPU;* **[FIG. 1, element 24: "L2 Cache Controller"]** *and a cache memory coupled to the cache controller and providing cache memory space to the CPU;* **[FIG. 1, element 44: "L2 Cache (Data)"]** *wherein the cache controller allows communication between the CPU and the bridge device when the CPU communicates using a first communication protocol and the bridge device communicates using a second communication protocol,* **[Herring discloses in column 2, lines 49-51, "An integrated L2 cache controller and local bus controller cooperate to support different protocols depending on whether L2 cache or local bus operation is required." See column 7, line 60 – column 8, line 5]** *and wherein the cache controller allows communication between the CPU and the bridge device when the CPU communicates using the second communication protocol and the bridge*

device communicates using the first communication protocol." **[Herring discloses in column 2, lines 49-51, "An integrated L2 cache controller and local bus controller cooperate to support different protocols depending on whether L2 cache or local bus operation is required." See column 7, line 60 – column 8, line 5]**

With respect to **claim 2**,

"The computer system of claim 1 wherein the cache controller comprises switch logic coupled between a first protocol interface and a second protocol interface, the switch logic implements a communication protocol to transfer information between the first protocol interface and the second protocol interface." **[Herring discloses this limitation, e.g. in column 7, lines 38-49 and column 7, line 60 – column 8, line 5]**

With respect to **claim 3**,

"The computer system of claim 2 wherein the communication protocol implemented by the switch logic is different from the first and second communication protocols." **[Herring discloses in column 6, lines 13-17, "...during L2-cache transfers, the clock speeds and handshake protocols on the PCI-bus 48 are not necessarily in conformance with the PCI protocol, but rather, are optimized along with other sideband signals, for fast L2 cache throughput."]**

With respect to **claim 4**,

"The computer system of claim 3 wherein the cache controller further comprises a cache memory interface coupled to the cache memory, **[disclosed in column 5, lines 27-28, "a high speed interface for an "off-chip" L2 cache 44 (with respect to the CPU 10)."]** *the cache memory interface is operable to access data stored in the cache memory according to address information provided to the cache controller."* **[FIG. 5]**

With respect to **independent claim 5**,

"A cache controller, comprising: a first interface operable to communicate to an external device using a first communication protocol; a second interface operable to communicate to an external device using a second communication protocol different than the first communication protocol; **[Herring discloses in column 2, lines 49-51, "An integrated L2 cache controller and local bus controller cooperate to support different protocols depending on whether L2 cache or local bus operation is required." See column 7, line 60 – column 8, line 5]** *and a cache memory interface coupled to the first and second interfaces,* **[FIGs. 2, 3, and 5]** *the cache memory interface controls reading and writing to a cache memory;* **[disclosed, e.g. in column 6, lines 25-28, "For reads or writes to the L2 cache 44, cache tag and control logic circuitry 46 looks up the address compare bits for the appropriate line and compare the bits to the address compare bits for the current cycle."]** *wherein the first interface selectively communicates to an external device being one of a CPU and a bridge device;* **[FIGs. 2, 3, and 5. Note FIG. 1 an "interface" connecting element 24 ("L2**

Cache Controller") to element 32 ("X-bus")] *wherein the second interface selectively communicates to an external device being one of a CPU and a bridge device."* **[FIGs. 2, 3, and 5. Note FIG. 1 an "interface" connecting element 24 ("L2 Cache Controller") to element 26, ("PCI Controller")]**

With respect to **claim 6**,

"The cache controller of claim 5 further comprising a control module coupled to the first and second ports, the control module is operable to receive a control signal to select that the first interface communicate to one of the CPU and the bridge device." **[See FIG. 7, elements 70, 72, 74, 76, and 78, and all associated text]**

With respect to **claim 7**,

"The cache controller of claim 6 wherein the control module is operable to receive a control signal to select that the second interface communicate to one of the CPU and the bridge device." **[See FIG. 7, elements 70, 72, 74, 76, and 78, and all associated text. See column 9, line 40 – column 10, line 35; Herring outlines various control modules ("control block") that select various interfaces to communicate with the CPU or bridge device.]**

With respect to **claim 8**,

"The cache controller of claim 5 wherein the cache memory interface determines whether address information from a CPU matches address tags in a tag memory." **[See FIGs. 2 and 3, element 46 and associated text]**

With respect to **claims 9 and 14,**

"The cache controller of claim 8 wherein, if the address information matches an address tag, **[Herring discloses in column 6, lines 28-30, "If there is a match, cache tag and control logic circuitry 46 drives the Hit signal active to indicate a match with the tag."]** *the cache controller provides data from the cache memory to the requesting CPU."*

With respect to **claims 10 and 15,**

"The cache controller of claim 8 wherein, if the address information does not match an address tag, the cache memory interface creates a new address tag and designates a memory location in a cache memory to store data associated with the address information." **[Herring teaches the limitations if this claim, e.g. in column 7, lines 50-54 and column 10, lines 2-5. Since a new line is being written to the L2 cache, a memory location is designated and an address tag is created.]**

With respect to **claim 11**,

"The cache controller of claim 8 wherein, if the address information does not match an address tag, the cache controller forwards the address information to a bridge device coupled to one of the first port and the second port." **[Herring teaches the limitations if this claim, e.g. in column 7, lines 50-54 and column 10, lines 2-5. When a cache "miss" occurs, the cache controller forwards the needed address information to a device that is coupled to the cache via a first or second interface port.]**

With respect to **independent claim 12**,

"A method, comprising: configuring a first port of a cache controller to communicate to an external device, wherein the first port selectively communicates to one of a CPU and a bridge device using a first communication protocol; **[See FIG. 5 and FIG. 7, elements 70, 72, 74, 76, and 78, and all associated text]** *and configuring a second port of the cache controller to communicate to an external device, wherein the second port selectively communicates to one of a CPU and a bridge device using a second communication protocol."* **[See FIG. 7, elements 70, 72, 74, 76, and 78, and all associated text. See column 9, line 40 – column 10, line 35; Herring outlines various control modules ("control block") that select various interfaces or ports to communicate with the CPU or bridge device.]**

With respect to **claim 13**,

"The method of claim 12 further comprising one of: configuring the first interface to communicate to a CPU and configuring the second interface to communicate to a bridge device; and configuring the first interface to communicate to a bridge device and configuring the second interface to communicate to a CPU." **[disclosed e.g. in column 3, lines 8-12,"...a specific example of a highly integrated central processing unit having L2 cache support employing a general purpose local bus separate from the CPU bus, such as, but not limited to, a PCI bus, without adhering to the local bus protocol, practiced in accordance with the present invention."]**

With respect to **independent claim 16**,

> *"A computer system, comprising: a central processing unit ("CPU");* **[FIG. 1, element 14: "CPU Core"]** *a bridge device coupled to a main memory;* **[FIG. 1, elements 20, 28, 32, 38: as interpreted by the examiner, these devices are a bridge device which is coupled to main memory ("System Memory" 36)]**

The following limitations of **claim 16** are interpreted under 35 U.S.C. 112, 6th paragraph.

According to the applicant's specification in paragraph [0018], the Examiner notes that the means or system/structure ("cache memory interface 116") for practice of the invention disclosed in the following limitation of Claim 16, is further taught in **Herring as follows:**

> *and means for reading and writing to a cache memory coupled between the CPU and the bridge device;* **[FIG. 1, element 24: "L2 Cache Controller"]** *wherein said means for reading and writing to the cache memory allows communication between the CPU and the bridge device* **[FIG. 1]** *when the CPU communicates using a first communication protocol* **[disclosed e.g. in column 3, lines 8-12,"...a specific example of a highly integrated central processing unit having L2 cache support employing a general purpose local bus separate from the CPU bus, such as, but not limited to, a PCI bus, without adhering to the local bus protocol, practiced in accordance with the present invention."]** *and the bridge device communicates using a second communication protocol, and allows communication between the CPU and the bridge device* **[FIG. 1]** *when the CPU communicates using the second communication protocol and the bridge device communicates using the first*

communication protocol." **[Herring discloses in column 2, lines 49-51, "An integrated L2 cache controller and local bus controller cooperate to support different protocols depending on whether L2 cache or local bus operation is required." See column 7, line 60 – column 8, line 5]**

With respect to **claim 17**,

"The computer system of claim 16 further comprising

The following limitations of **claim 16** are interpreted under 35 U.S.C. 112, 6th paragraph.

According to the applicant's specification in paragraph [0018], the Examiner notes that the means or system/structure ("cache memory interface 116") for practice of the invention disclosed in the following limitation of Claim 16, is further taught in **Herring as follows:**

means for determining whether address information from a CPU request matches an address tag stored in the cache controller." **[Herring discloses in column 6, lines 28-30, "If there is a match, cache tag and control logic circuitry 46 drives the Hit signal active to indicate a match with the tag."]**

With respect to **claim 18**,

"The computer system of claim 17 further comprising

The following limitations of **claim 16** are interpreted under 35 U.S.C. 112, 6th paragraph.

According to the applicant's specification in paragraph [0018], the Examiner notes that the means or system/structure ("cache memory interface 116") for practice of the invention disclosed in the following limitation of Claim 16, is further taught in **Herring as follows:**

means for accessing data stored in the cache memory if the address information matches an address tag." **[As stated supra, this limitation is notoriously well know to persons of ordinary skill in the art]**

With respect to **claim 19**,

"The computer system of claim 17 further comprising

The following limitations of **claim 16** are interpreted under 35 U.S.C. 112, 6th paragraph.

According to the applicant's specification in paragraph [0018], the Examiner notes that the means or system/structure ("cache memory interface 116") for practice of the invention disclosed in the following limitation of Claim 16, is further taught in **Herring as follows:**

means for creating a new address tag for association with the address information and designating a memory location in the cache memory for storing data associated with the address information if the address information does not match an address tag." **[Herring teaches the limitations if this claim, e.g. in column 7, lines 50-54 and column 10, lines 2-5. Since a new line is being written to the L2 cache, a memory location is designated and an address tag is created:]**

With respect to **independent claims 20 and 24, and claim 21,**

"A cache controller, **[FIG. 1, element 24: "L2 Cache Controller"]** *comprising: a plurality of first communication protocol interfaces that allow communication between the cache controller and at least one of a processor and a bridge device, wherein each of the processor and bridge device communicates using a first communication protocol;* **[FIG. 1, elements 24 and 26. See associated text for FIG. 1 Also taught in column 2, lines 40-54.]** *and a plurality of second communication protocol interfaces that allow communication between the cache controller and at least one of a processor and a bridge device, wherein each of the processor and bridge device communicates using a second communication protocol."* **[FIG. 1, elements 24 and 26. See associated text for FIG. 1. Also taught in column 2, lines 40-54.]**

With respect to **claim 22,**

"The computer system of claim 20 wherein the cache controller comprises a control unit coupled to the plurality of ports, **[See FIG. 7 and associated text]** *the control unit operable to configure the ports according to a control signal* **[FIG. 6]** *such that the cache controller allows one of: communication between the CPU and the bridge device when the CPU and the bridge device communicate using a first communication protocol; communication between the CPU and the bridge device when the CPU and the bridge device communicate using a second communication protocol;* **[See FIG. 7, elements 70, 72, 74, 76, and 78, and all associated text. See column 9, line 40 – column 10, line 35; Herring**

outlines various control modules ("control block") that select various interfaces or ports to communicate with the CPU or bridge device.] *communication between the CPU and the bridge device when the CPU communicates using the first communication protocol and the bridge device communicates using the second communication protocol; and communication between the CPU and the bridge device when the CPU communication using the second communication protocol and the bridge device communicates using the first communication protocol."* **[Herring teaches these limitations, e.g. in column 2, lines 40-54.] [Herring also discloses this limitation, e.g. in column 3, lines 8-13]**

With respect to **independent claim 23**,

"A computer system, comprising: a central processing unit ("CPU"); **[FIG. 1, element 14: "CPU Core"]** *a bridge device coupled to a main memory;* **[FIG. 1, element 26: as interpreted by the examiner, these devices are a bridge device which is coupled to main memory ("System Memory" 36)]** *a cache controller coupled between the bridge device and the CPU;* **[FIG. 1, element 24: "L2 Cache Controller"]** *and a cache memory coupled to the cache controller and providing cache memory space to the CPU;* **[FIG. 1, element 44: "L2 Cache (Data)"]** *wherein the cache controller allows communication between the CPU and the bridge device when the CPU and the bridge device communicate using different communication protocols,* **[Herring discloses in column 2, lines 49-51, "An integrated L2 cache controller and local bus controller cooperate to support different protocols depending on whether L2 cache or local bus**

operation is required." See column 7, line 60 – column 8, line 5] *and wherein the cache controller also allows communication between the CPU and the bridge device when the communication protocols of the CPU and bridge device are reversed."* **[Herring discloses in column 8, lines 17-26,"The PCI Owns Bus signal is active if the PCI controller 26 is currently operating in PCI protocol or if there are cycles pending to the PCI-bus 48 from a PCI compliant device. While the PCI Owns Bus signal is active, the L2 cache controller 24 cannot begin cycles to the L2 cache 44. Any cacheable addresses on the X-bus 32 that occur while the PCI Owns Bus signal is active will be queued by the L2 cache controller 24 until the PCI Owns Bus signal goes inactive and the PCI-bus 48 can revert to L2 cache protocol."]**

With respect to **claim 25**,

"The computer system as defined in claim 24 wherein each of the processor **[FIG. 1, element 14: "CPU Core"]** *and the bridge device are coupled to the plurality of first communication protocol interfaces."* **[FIG. 1, elements 24 and 26. See associated text for FIG. 1. Also taught in column 2, lines 40-54.]**

With respect to **claim 26**,

"The computer system as defined in claim 24 wherein each of the processor **[FIG. 1, element 14: "CPU Core"]** *and the bridge device are coupled to the plurality of second communication protocol interfaces."* **[FIG. 1, elements 24 and 26. See associated text for FIG. 1. Also taught in column 2, lines 40-54.]**

With respect to **claim 27**,

> *"The computer system as defined in claim 24 wherein the processor* **[FIG. 1, element 14: "CPU Core"]** *is coupled to one of the first communication protocol interfaces, and the bridge device is coupled to one of the second communication protocol interfaces."* **[disclosed, e.g. in column 2, lines 40-54.]**

With respect to **claim 28**,

> *"The computer system as defined in claim 24 wherein each of the processor* **[FIG. 1, element 14: "CPU Core"]** *and the bridge device are coupled to the plurality of second communication protocol interfaces."* **[FIG. 1, elements 24 and 26. See associated text for FIG. 1. Also taught in column 2, lines 40-54.]**

CONCLUSION

Direction of Future Correspondences

Any inquiry concerning this communication or earlier communication from the examiner should be directed to Horace L. Flournoy whose telephone number is (571) 272-2705. The examiner can normally be reached on Monday through Friday 8:00 AM to 5:30 PM (ET).

Important Note

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Reginald G. Bragdon can be reached on (571) 272-4204. The fax phone numbers for the organization where this application or proceeding is assigned is (703) 746-7239.

Information regarding the status of an Application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or PUBLIC PAIR. Status information for unpublished applications is available through Private Pair only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is (571) 272-2100.

Reginald G. Bragdon
REGINALD G. BRAGDON
PRIMARY EXAMINER

Horace L. Flournoy

Patent Examiner

Art unit: 2189

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Technology Center 2100